IN THE CLAIMS

Claims 1-28 were pending. Claims 1, 4-8, 12, 14, 17-18, 20-22, 24, 26, and 28 have been amended. Claims 3, 13, 19, and 25 have been canceled without prejudice. Claims 1-2, 4-12, 14-18, 20-24, and 26-28 remain pending. A complete list of claims is presented below with amendments marked up:

Current Listing of Claims:

1.   (Currently amended) A method to manage power in a system, the method comprising:

monitoring transactions over an interconnect coupling a chipset device and a peripheral device in the system, the transactions being transmitted between the peripheral device and the chipset device according to a flow control protocol that allows the chipset device to keep track of the transactions; ~~and~~

causing a processor in the system to exit from a power state if a plurality of coherent transactions pending in a buffer of the chipset device exceeds a first threshold; and

de-asserting an indicator within a message packet to allow the processor to enter into the power state in response to a request from the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the chipset device exceeds a second threshold.

2.   (Original) The method of claim 1, further comprising:

determining whether a predetermined period of time has passed if the plurality of

coherent transactions pending in the buffer does not exceed the first threshold; and

causing the processor to exit from the power state if the predetermined period of

time has passed.

3.   (Canceled).

4.   (Currently amended) The method of claim [[3]] 1, further comprising:

asserting the indicator within the message packet to prevent the processor from

entering the power state if the plurality of incoherent transactions pending in the buffer of

the chipset device exceeds the second threshold.

5.   (Currently amended) The method of claim [[3]] 1, further comprising:

determining whether a second predetermined period of time has passed if the

plurality of incoherent transactions pending in the buffer of the chipset device is below

the second threshold; and

deasserting the indicator within the message packet to allow the processor to enter

the power state if the second predetermined period of time has passed.

6.   (Currently amended) The method of claim [[3]] 1, wherein the first threshold is

substantially equal to the second threshold.

7.   (Currently amended) The method of claim [[3]] 1, wherein the first threshold is

lower than the second threshold.

8.   (Currently amended) The method of claim [[3]] 1, wherein the first threshold is

higher than the second threshold.

9.   (Original) The method of claim 1, wherein the flow control protocol is Peripheral

Component Interconnect (PCI) Express.

10.   (Original) The method of claim 1, wherein the chipset device comprises a memory

controller.

11.   (Original) The method of claim 1, wherein the chipset device comprises an

input/output controller.

12.   (Currently amended) An apparatus in a computing system, the apparatus

comprising:

        power management circuitry to monitor transactions over an interconnect

coupling a root complex device and a peripheral device in the computing system, the

transactions being transmitted between the peripheral device and the root complex device

according to a flow control protocol to allow the root complex device to keep track of the

transactions transmitted; and

        a digital media interface coupled to the root complex device to send a first

message packet to the root complex device to cause a processor in the computing system

to exit from a power state if a plurality of coherent transactions pending in a buffer of the

root complex device exceeds a first threshold, wherein in response to a request from the

processor to enter into the power state, the power management circuitry de-asserts an indicator within a second message packet to allow the processor to enter into the power state if a plurality of incoherent transactions pending in the buffer of the root complex device exceeds a second threshold.

13.   (Canceled).

14.   (Currently amended) The apparatus of claim [[13]] 12, wherein in response to the request from the processor, the power management circuitry asserts the indicator within the second message packet to prevent the processor from entering the power state if the plurality of incoherent transactions pending in the buffer of the root complex device is below the second threshold.

15.   (Original) The apparatus of claim 14, further comprising a timer, wherein the power management circuitry asserts the indicator within the second message packet to prevent the processor from entering the power state if the timer has expired.

16.   (Original) The apparatus of claim 14, wherein the first threshold is substantially equal to the second threshold.

17.   (Currently amended) The apparatus of claim 12, wherein the flow control protocol is Peripheral Component Interconnect (PCI) Express includes a credit-based flow control accounting scheme.

18.   (Currently amended) A semiconductor chip in a computing system, the

semiconductor chip comprising:

a memory controller coupled to a peripheral device in the computing system;

power management circuitry coupled to the memory controller to monitor

transactions between the peripheral device and the memory controller; and

an input/output controller residing on a common substrate with the memory

controller to allow a processor in the computing system to enter into the power state in

response to a request from the processor to enter into a power state if a plurality of

incoherent transactions pending in a buffer of the memory controller exceeds an entry

threshold, [[and]] to prevent the processor from entering into the power state if the

plurality of incoherent transactions is below the entry threshold, and to cause the

processor to exit from the power state if a plurality of coherent transactions pending in the

buffer of the memory controller exceeds an exit threshold.

19.   (Canceled).

20.   (Currently amended) The semiconductor chip of claim [[19]] 18, wherein the

entry threshold is substantially equal to the exit threshold.

21.   (Currently amended) The semiconductor chip of claim [[19]] 18, wherein the

entry and exit thresholds are adaptively modifiable.

22.   (Currently amended) The semiconductor chip of claim 18, wherein the peripheral

device is coupled to the memory controller via an ~~a Peripheral Component Interconnect~~

~~(PCI)~~ ~~Express~~ interconnect, <u>which adopts a credit-based flow control accounting scheme</u>.

23.   (Original) The semiconductor chip of claim 18, wherein the peripheral device is

coupled to the memory controller via a bus.

24.   (Currently amended) A system comprising:

        a processor;

        a memory controller coupled to the processor;

        a graphics chip;

        an interconnect coupling the graphics chip to the memory controller;

        an input/output controller, coupled to the memory controller, comprising

                power management circuitry to monitor transactions over the interconnect,

the transactions being transmitted between the graphics chip and the memory controller

according to a flow control protocol; and

                a digital media interface coupled to the memory controller to send a first

message packet to the memory controller to cause the processor to exit from a power state

if a plurality of coherent transactions pending in a buffer of the memory controller

exceeds a first threshold, <u>wherein the power management circuitry de-asserts an indicator</u>

<u>within the second message packet in response to a request from the processor to enter into</u>

<u>the power state to allow the processor to enter into the power state if a plurality of</u>

<u>incoherent transactions pending in the buffer of the memory controller exceeds a second</u>

<u>threshold</u>.

25.   (Canceled).

26.   (Currently amended) The system of claim [[25]] 24, wherein the power

management circuitry asserts the indicator within the second message packet in response

to the request from the processor to prevent the processor from entering the power state if

the plurality of incoherent transactions pending in the buffer of the memory controller is

below the second threshold.

27.   (Original) The system of claim 26, wherein the first threshold is substantially

equal to the second threshold.

28.   (Currently amended) The system of claim 24, wherein the flow control protocol is

Peripheral Component Interconnect (PCI) Express includes a credit-based flow control

accounting scheme.